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The disclosure was objected to as including an informality on page 5. The disclosure has been amended in response to the objection.

The abstract was objected to as not having a length within the range of 50 to 150 words. The abstract has been amended in response to the objection.

Claim 12 was objected to as including various informalities. Claim 12 has been amended in response to the objection.

Claims 1-4 and 7-11 stand rejected under 35 U.S.C. 112, second paragraph. Claims 1, 4, 7, 8, 9, and 11 have been amended in response to the rejection.

Claims 1-12 stand rejected under 35 U.S.C. 102(b) as being anticipated by Rostoker, et al. (U.S. Patent No. 5,838,163). Applicant respectfully traverses the rejection. Claim 1, as amended, includes the features of "at least one probe pad; multiple test structures which are selectably multiplexed to said probe pad in dependence on a voltage applied thereto." Rostoker does not disclose such features. Rostoker, in Figures 4a and 4b, relies on control signals 445 to select among several scribe line conductors 420. Rostoker does not teach or suggest selectably multiplexing to probe pad 440 through applying a particular voltage to pad 440. The Examiner refers to bonding pads connected to control signals 445, but Applicant disagrees with the Examiner's interpretation of Rostoker's figure. The dots at the ends of control signals 445 are not bond pads, but are rather part of the standard representation of a switch. It is clear from Rostoker (col. 12, lines 19-23) that selection among the various scribe line conductors is made by applying a voltage to control signals 445, not to probe pad 440. Therefore, Applicant respectfully submits that Claim 1 is patentable over Rostoker.

Claim 2 includes the limitation "wherein said probe pad is located in a scribeline, and occupies more than half the width of said scribeline." The rejection is based on Rostoker's Figure 4b. Figure 4b gives no indication that the

shown structure is in a scribeline, and, even if the area shown is in a scribeline, probe pad 440 clearly does not occupy more than half the width thereof. Claims 3 and 4 depend from Claim 1 and are therefore patentable for at least the reasons presented above for that claim.

Claim 5 includes the feature of "at least one probe pad in a scribeline; multiple test structures in said scribeline which are all physically close to said probe pad, and which are selectably multiplexed to said probe pad in dependence on at least one global input." Rostoker does not disclose multiple test structures in the same scribeline as a probe pad. The elements labeled "420" in Rostoker's Figures 4a and 4b are "scribe line conductors" which originate at discrete, individual die on the wafer and terminate in a common area (col. 12, lines 1-5). Rostoker does not indicate that any of the features in Figures 4a and 4b are within a scribeline. In addition, it is clear from Rostoker's description of the scribe line conductors that they are attached to test structures outside any scribe line in various die on the wafer. Therefore, Applicant respectfully submits that Claim 5 is patentable over Rostoker.

Claim 6 includes the feature "wherein said probe pad occupies more than half the width of said scribeline." Rostoker's Figure 4b gives no indication that the shown structure is in a scribeline, and, even if the area shown is in a scribeline, probe pad 440 clearly does not occupy more than half the width thereof. Claims 7 and 8 depend from Claim 5 and are therefore patentable for at least the reasons presented above for that claim.

Claim 9 includes the features of a test selector circuit located in a single scribeline portion, as well as multiple test structures and a probe pad located in the scribeline portion. The test selector circuit operates in dependence upon a voltage applied at the probe pad. Rostoker does not disclose such features. The rejection is based on Rostoker's Figure 4b, but that figure is not indicated as being in a scribeline. Also, Rostoker, in Figures 4a and 4b, relies on control signals 445 to select among several scribe line conductors 420. That reference

does not rely upon voltage applied to probe pad 440. Therefore, Applicant submits that Claim 9 is patentable over Rostoker.

Claim 10 includes the feature "wherein said probe pad occupies more than half the width of said scribeline." Rostoker's Figure 4b gives no indication that the shown structure is in a scribeline, and even if the area shown is in a scribeline, probe pad 440 clearly does not occupy more than half the width thereof. Claim 11 depends from Claim 9 and is therefore patentable for at least the reasons presented above for that claim.

Claim 12 includes the step of "applying a selection signal to a probe pad coupled to said multiple test structures, to drive a selector circuit to connect a selected one of said multiple test structures to said pad." It is clear from Rostoker (col. 12, lines 19-23) that selection among the various scribe line conductors is made by applying a voltage to control signals 445, not to probe pad 440. Therefore, Applicant respectfully submits that Claim 12 is patentable over Rostoker.

Applicant respectfully requests reconsideration and withdrawal of the rejections and allowance of Claims 1-12. If the Examiner has any questions or other correspondence regarding this application, Applicant requests that the Examiner contact Applicant's attorney at the below listed telephone number and address.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification:

On page 5, in the paragraph beginning at line 108:

--Advantages of the disclosed methods and structures, in various embodiments, can include one or more of the following:
-more test structures can be made larger;
-quicker correction of process deviations;
-increased efficiency of use of wafer area;
-increased efficiency of use of scribeline area;
-fewer probe pads are needed;
-increased yield;
-increased capability for "early warning" testing increases reliability of the integrated circuits[;].--

In the Abstract:

A test selector that multiplexes different test structures (202) to an adjacent probe pad (206) in dependence on the probe voltage. In addition, a scribeline test circuit is disclosed that includes a test selector circuit located in a single scribeline portion between two adjacent die locations. Multiple test structures and at least one probe pad also are located in the single scribeline portion. The test selector circuit makes an electrical connection from the probe pad to a selected one of the test structures depending upon a voltage applied at the probe pad.

In the Claims:

1. (amended) A partially fabricated wafer, comprising:

at least one probe pad;

multiple test structures which are selectably multiplexed to said probe pad in dependence on a [the] voltage applied thereto.

4. (amended) The wafer of Claim 1, wherein said multiple test structures are selectively multiplexed to said probe pad in dependence on a [the] sequence of voltages applied to said probe pad.

5. (amended) A partially fabricated wafer including die separated by scribelines, comprising:

at least one probe pad in a scribeline;

multiple test structures in said scribeline which are all physically close to said probe pad, and which are selectably multiplexed to said probe pad in dependence on at least one global input.

6. (amended) The wafer of Claim 5, wherein said probe pad [is located in a scribeline, and] occupies more than half the width of said scribeline.

7. (amended) The wafer of Claim 5, wherein said multiple test structures are selectively multiplexed to said probe pad in dependence on a [the] voltage applied to said probe pad.

8. (amended) The wafer of Claim 5, wherein said multiple test structures are selectively multiplexed to said probe pad in dependence on a [the] sequence of voltages applied to said probe pad.

9. (amended) A scribeline test circuit, comprising:

a test selector circuit located in a single scribeline portion between two adjacent die locations;

multiple test structures, also located in said single scribeline portion; and

at least one probe pad, also located in said single scribeline portion;

wherein said test selector circuit makes an electrical connection from said probe pad only to a selected one of said test structures, in dependence on a [the] voltage applied at said probe pad.

11. (amended) The circuit of Claim 9, wherein said multiple test structures are selectively multiplexed to said probe pad in dependence on a [the] sequence of voltages applied to said probe pad.

12. (amended) A method for characterizing [testing] integrated circuits using multiple test structures, comprising the steps of:

(a.) applying a selection signal to a probe pad coupled to said multiple test structures, to drive a selector circuit to connect a selected one of said multiple test structures to said pad [paid]; and

(b.) applying a controlled voltage to said pad, and thereby measuring the electrical characteristics of the selected one of said multiple test structures.